ABSTRACT OF THE DISCLOSURE

An apparatus is disclosed which includes a converter circuit and a noise suppression circuit. The converter circuit has a dynamic logic input, and is configured to generate a static logic output on an output node responsive to the dynamic logic input. The noise suppression circuit is coupled to receive a clock signal and is coupled to the output node. Responsive to a first phase of the clock signal, a precharge of a dynamic logic circuit generating the dynamic logic input occurs. The noise suppression circuit is configured to actively drive the static logic output on the output node responsive to the first phase. In some embodiments, the noise suppression circuit may reduce the noise sensitivity of the static logic output during the precharge phase, and may not impede operation of the converter circuit during the evaluate phase.